The Optimal SMA Chipset for Mobile PC Applications

February, 2001
Platform Conference

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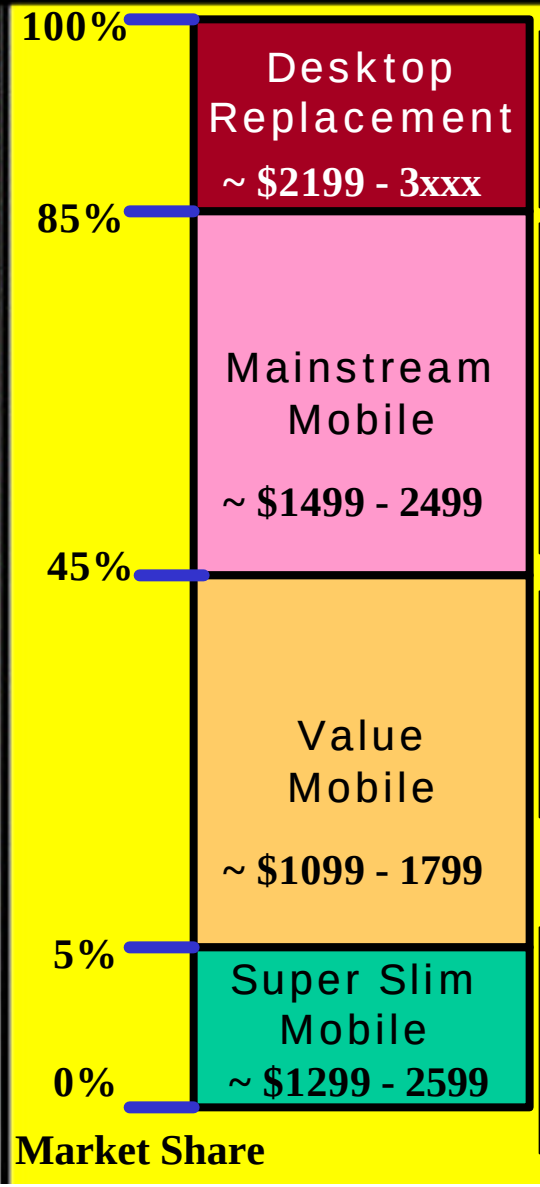
Mobile PC Market Segment Survey



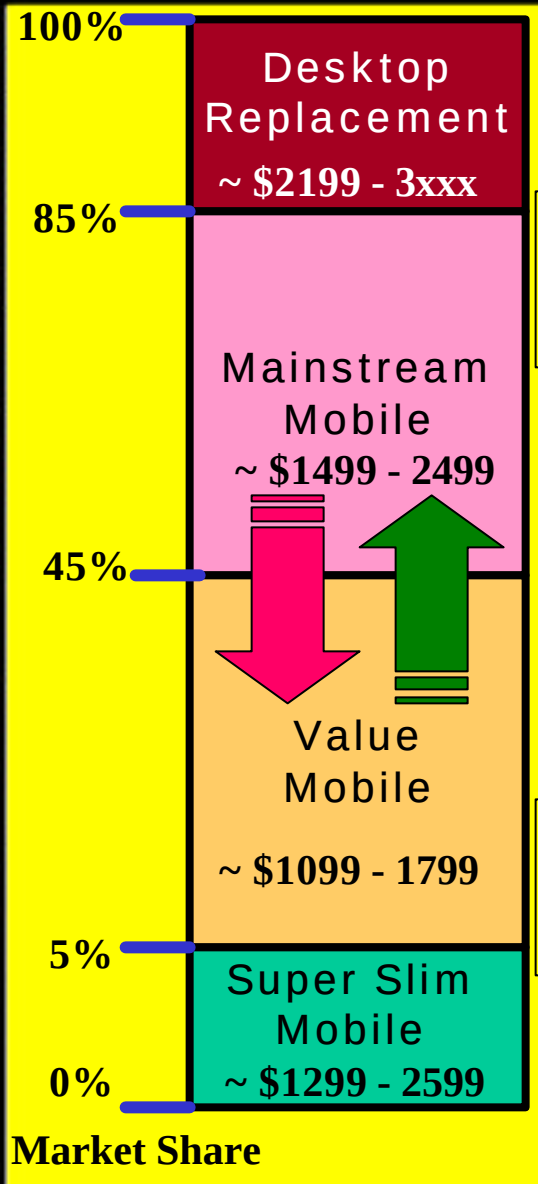
- New technologies, Better Thermal handling
- All-in-One, Full Featured, High Performance,
- Trade-off for travel weight, Battery life

- Selling on CPU MHz, DRAM, HD, TFT size and Battery life
- All-in-one, Full Featured, 2D performance
- Corporate buyer: Biz application, 2D Performance and Docking
- Consumer buyer: 3D and DVD/full frame rate
- Networking:Ethernet and Modem build-in

- Out-dated models from mainstream, Less on CPU MHz, DRAM, HD, TFT size
- Consumer buyer: 2D and CD-ROM, DVD optional
- Modem built-in or PCMCIA

- Selling on Weight and Battery life
- Must buy Accessories and small TFT
- Corporate buyer: Japan market
- Networking or Modem build-in

Mobile PC Segment Consolidation



- Pricing pressure: Mainstream under $2K
- Faster/larger/bigger/connected
- Less travel weight and longer battery life

TWISTER

The Optimal solution for the dynamic mobile market

- New pricing benchmark: under $1K mobile
- Full featured, Speeded/TFT, acceptable performance
- Dynamic market window, shorter product life span

Twister PN/KN133 SMA Mobile Chipset Overview

Highly Integrated Mobile chipset with extra value

System ASP($)

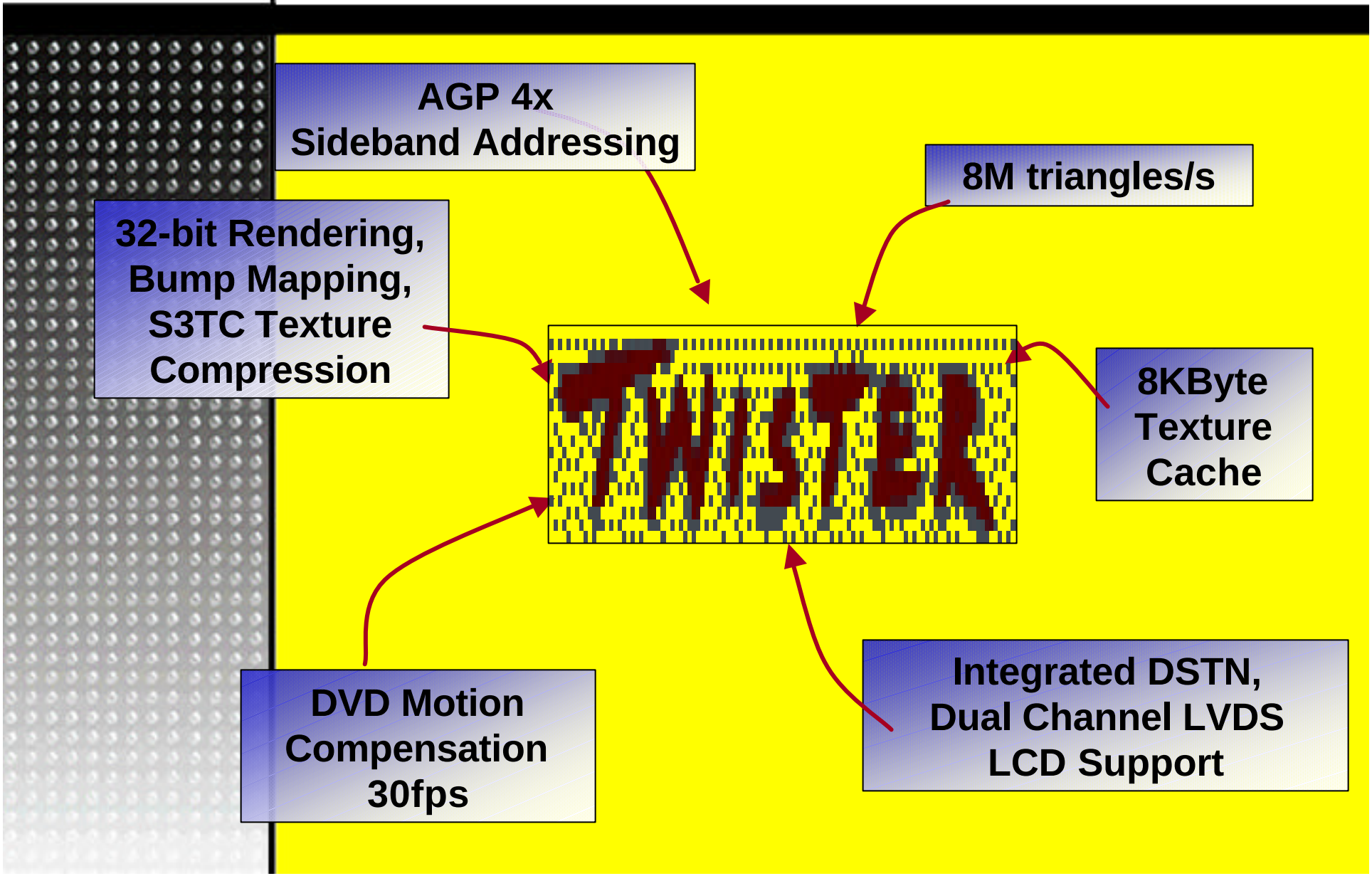
$1999

Value Mobile PC 2001

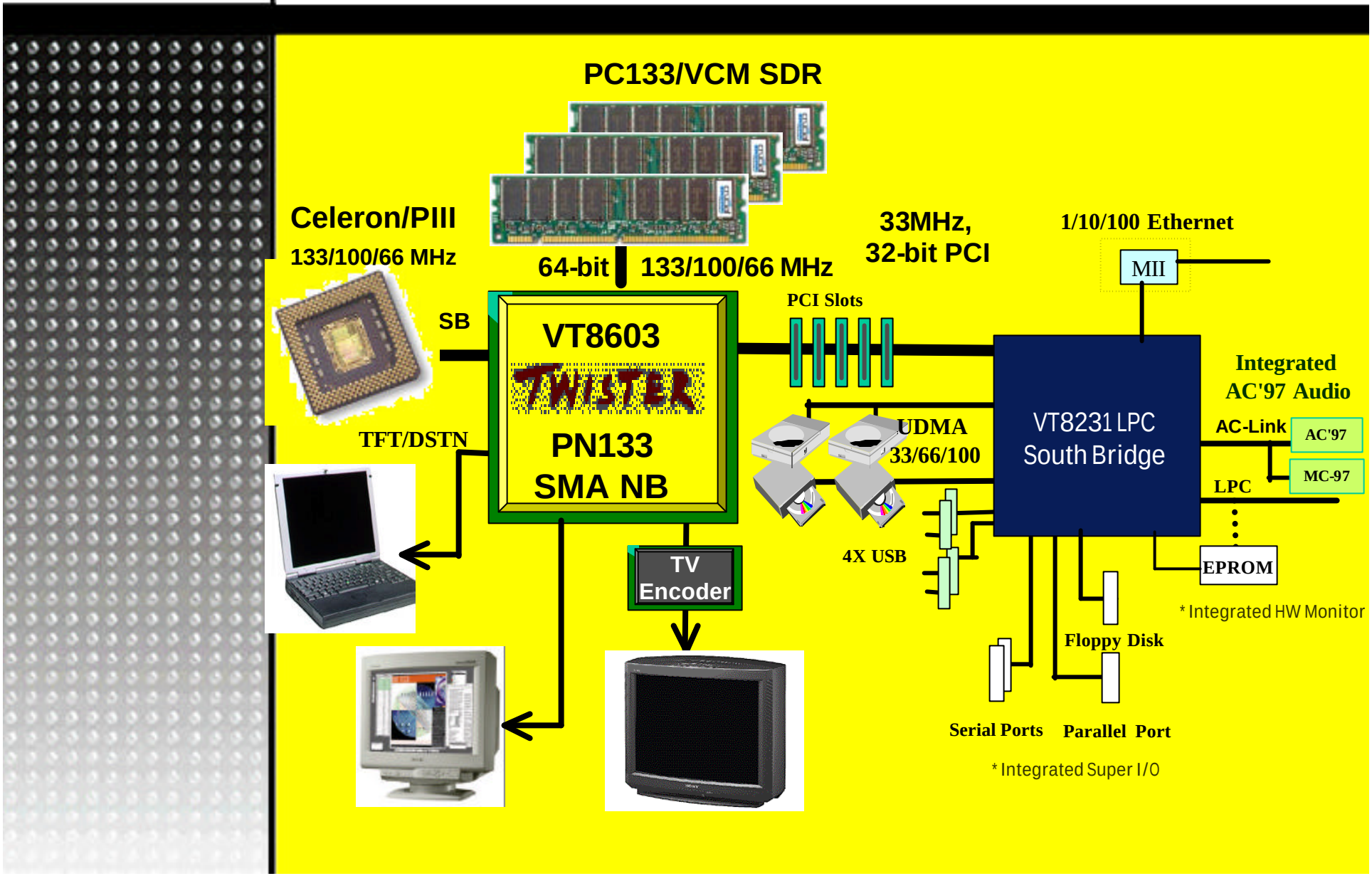
$1000

- Twister features:
  - Support P6 FSB 66-133 MHz with PN133
  - Support for Athlon FSB 200-266MHz with KN133
  - PC133 SMA System Memory
  - Integrated Savage4 graphics 2D/3D core
  - Integrated DSTN and LVDS support
  - Advanced Power Management controls
  - 33 MHz, 32-bit PCI
- SMA NB eliminates separate graphics subsystem, with excellent 2D and 3D performance
- Multiple PCI South Bridge Options address Commercial and Consumer requirements

Twister Graphics Core Overview

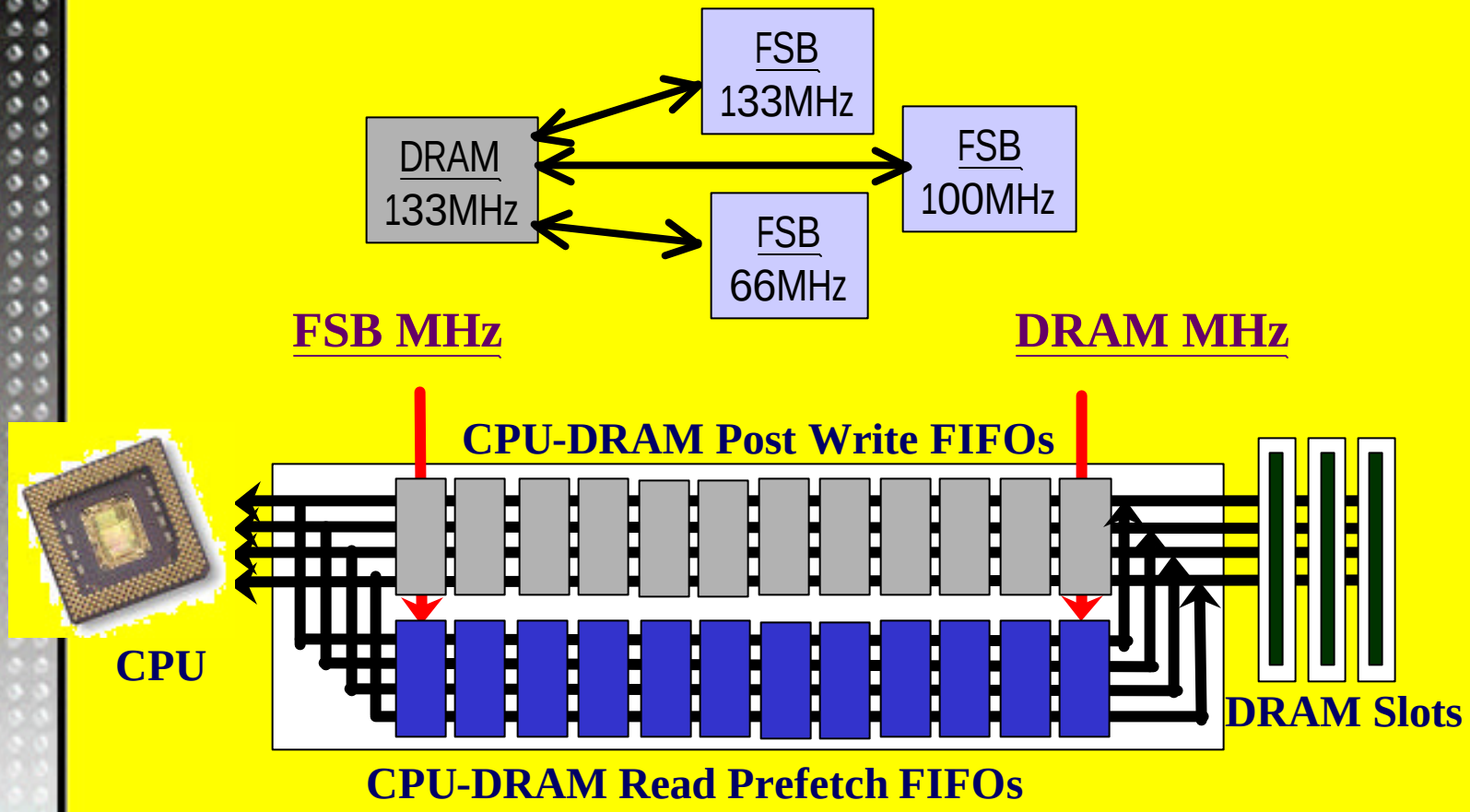


ProSavage Twister SMA Mobile System Partition



Twister Architecture: Flexibility and Scalable

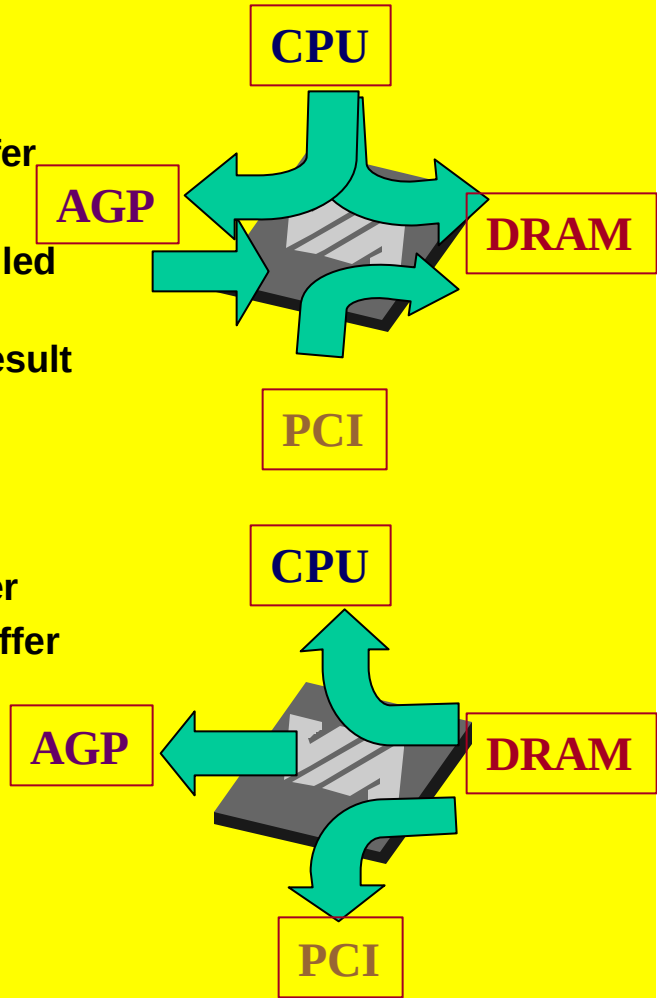
Pseudo/Synchronous CPU/DRAM interface



Enhancements Buffer Management

"Built-in multiple FIFOs to optimal data movement concurrency "

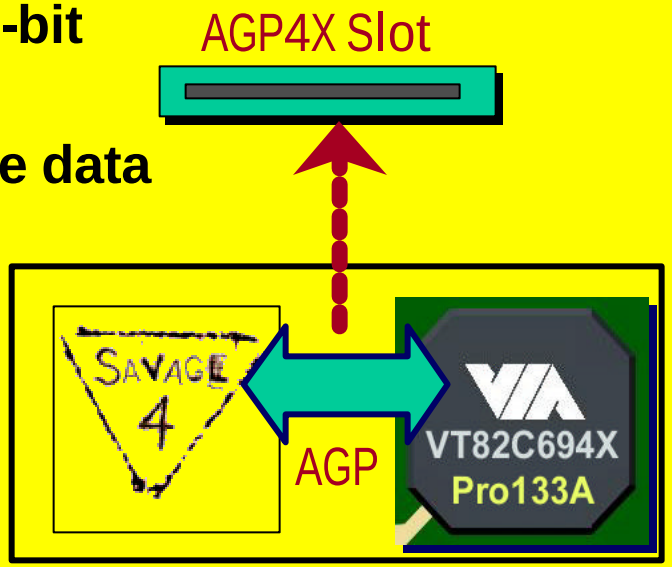
- **CPU-to-DRAM FIFOs**
  - 16 QWs of CPU to DRAM post write buffer
  - 16 QWs of CPU read prefetch buffer
  - Read-Around-Write capable for non-stalled CPU reads
  - Speculative DRAM read before snoop result
- **CPU-to-PCI FIFOs**
  - 64 DWs of CPU to PCI post write buffer
  - Byte merging in CPU-PCI write buffer
  - 32 DWs of PCI to DRAM post write buffer
  - 16 DW of PCI to DRAM read prefetch buffer
- **AGP4X/2X FIFOs with Fast-Write**
  - 32 QWs read data buffer
  - 16 QWs write data buffer
- **Deep Display Prefetch Queue**



Internal AGP High Speed Data Path

SW and Driver transparent vs AGP External device

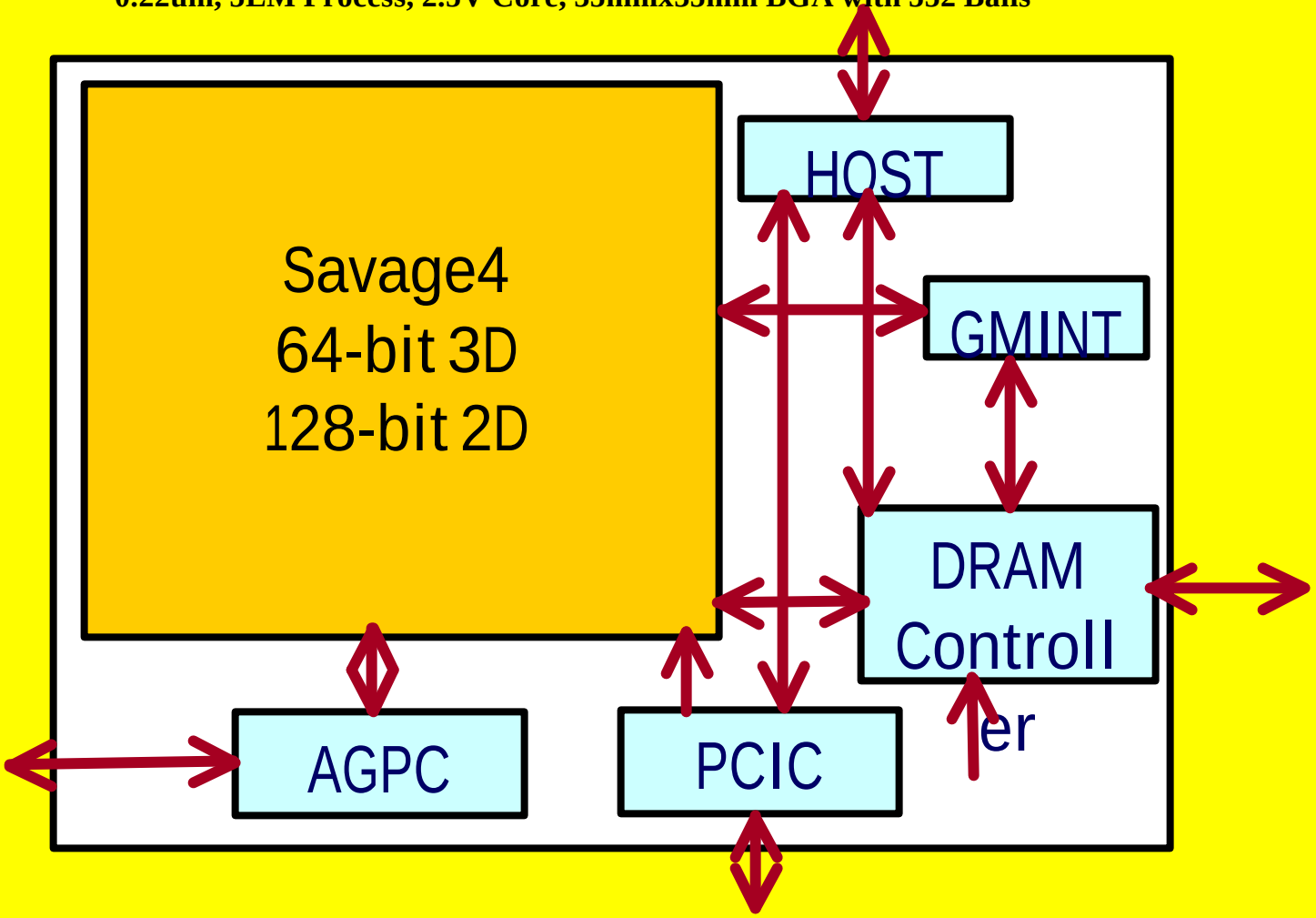
- **Integrated Savage4 Graphics Core**
  - **66MHz AGP CLK with 128-bit data path**
  - **wider internal bus improve data throughput**
- **Compliant to AGP2.0**
- **Eliminate External Graphics Subsystem**
  - **Save PCB Real Estate**
  - **Reduce Power Consumption**



Twister Die/Gate Count Utilization

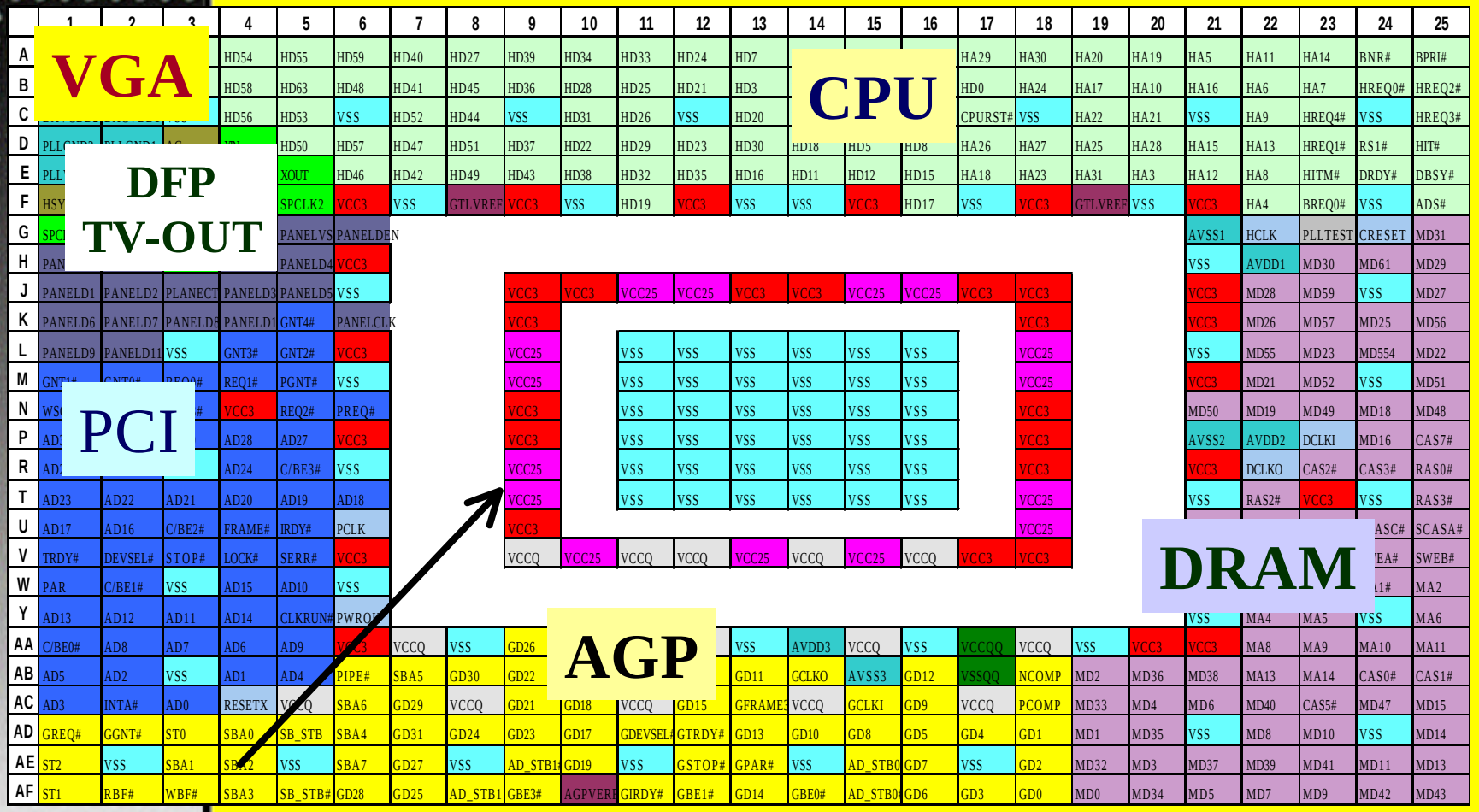
A Balanced PAD/Core ASIC Design

0.22um, 5LM Process, 2.5V Core, 35mmx35mm BGA with 552 Balls



A Balanced Core/Pad Design

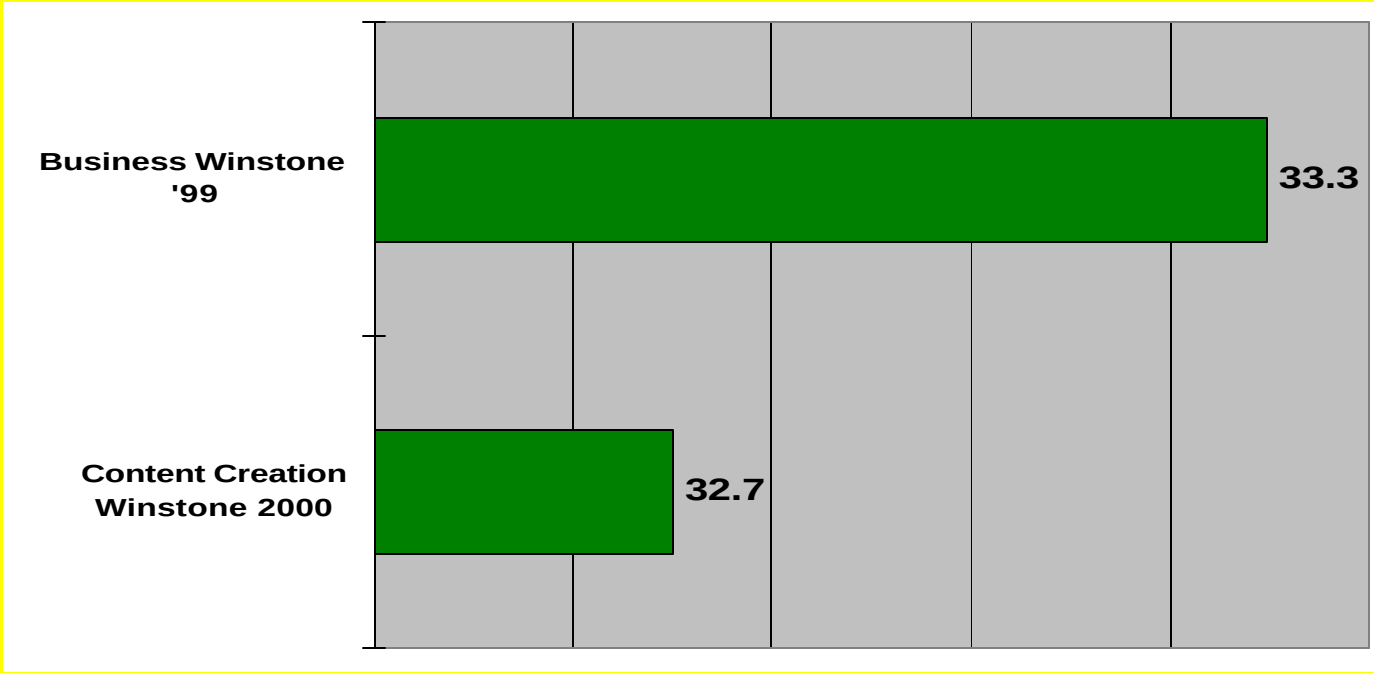
0.22uM, 2.5V Core and 35x35mm, 552 BGA Package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A				HD54	HD55	HD59	HD40	HD27	HD39	HD34	HD33	HD24	HD7				HA29	HA30	HA20	HA19	HA5	HA11	HA14	BNR#	BPRI#
B				HD58	HD63	HD48	HD41	HD45	HD36	HD28	HD25	HD21	HD3				HD0	HA24	HA17	HA10	HA16	HA6	HA7	HREQ0#	HREQ2#
C				HD56	HD53	VSS	HD52	HD44	VSS	HD31	HD26	VSS	HD20				CPURST#	VSS	HA22	HA21	VSS	HA9	HREQ4#	VSS	HREQ3#
D	PLLGND2	PLLGND1	AC		HD50	HD57	HD47	HD51	HD37	HD22	HD29	HD23	HD30	HD18	HD5	HD8	HA26	HA27	HA25	HA28	HA15	HA13	HREQ1#	RS1#	HIT#
E	PLL				XOUT	HD46	HD42	HD49	HD43	HD38	HD32	HD35	HD16	HD11	HD12	HD15	HA18	HA23	HA31	HA3	HA12	HA8	HITM#	DRDY#	DBSY#
F	HSY				SPCLK2	VCC3	VSS	GTLVREF	VCC3	VSS	HD19	VCC3	VSS	VSS	VCC3	HD17	VSS	VCC3	GTLVREF	VSS	VCC3	HA4	BREQ0#	VSS	ADS#
G	SPCI				PANELVS	PANELDEN															AVSS1	HCLK	PLLTEST	CRESET	MD31
H	PAN				PANELD4	VCC3															VSS	AVDD1	MD30	MD61	MD29
J	PANELD1	PANELD2	PLANECT	PANELD3	PANELD5	VSS			VCC3	VCC3	VCC25	VCC25	VCC3	VCC3	VCC25	VCC25	VCC3	VCC3			VCC3	MD28	MD59	VSS	MD27
K	PANELD6	PANELD7	PANELD8	PANELD1	GNT4#	PANELCLK			VCC3									VCC3			VCC3	MD26	MD57	MD25	MD56
L	PANELD9	PANELD11	VSS	GNT3#	GNT2#	VCC3			VCC25		VSS	VSS	VSS	VSS	VSS	VSS		VCC25			VSS	MD55	MD23	MD554	MD22
M	GNT1#	GNT0#	REQ0#	REQ1#	PGNT#	VSS			VCC25		VSS	VSS	VSS	VSS	VSS	VSS		VCC25			VCC3	MD21	MD52	VSS	MD51
N	WS		#	VCC3	REQ2#	PREQ#			VCC3		VSS	VSS	VSS	VSS	VSS	VSS		VCC3			MD50	MD19	MD49	MD18	MD48
P	AD			AD28	AD27	VCC3			VCC3		VSS	VSS	VSS	VSS	VSS	VSS		VCC3			AVSS2	AVDD2	DCLKI	MD16	CAS7#
R	AD			AD24	C/BE3#	VSS			VCC25		VSS	VSS	VSS	VSS	VSS	VSS		VCC3			VCC3	DCLKO	CAS2#	CAS3#	RAS0#
T	AD23	AD22	AD21	AD20	AD19	AD18			VCC25		VSS	VSS	VSS	VSS	VSS	VSS		VCC25			VSS	RAS2#	VCC3	VSS	RAS3#
U	AD17	AD16	C/BE2#	FRAME#	IRDY#	PCLK			VCC3									VCC25						ASC#	SCASA#
V	TRDY#	DEVSEL#	STOP#	LOCK#	SERR#	VCC3			VCCQ	VCC25	VCCQ	VCCQ	VCC25	VCCQ	VCC25	VCCQ	VCC3	VCC3						EA#	SWEB#
W	PAR	C/BE1#	VSS	AD15	AD10	VSS																			
Y	AD13	AD12	AD11	AD14	CLKRUN#	PWRO															VSS	MA4	MA5	VSS	MA6
AA	C/BE0#	AD8	AD7	AD6	AD9	VCC3	VCCQ	VSS	GD26					VSS	AVDD3	VCCQ	VSS	VCCQQ	VCCQ	VSS	VCC3	VCC3	MA8	MA9	MA10	MA11
AB	AD5	AD2	VSS	AD1	AD4	PIPE#	SBA5	GD30	GD22					GD11	GCLKO	AVSS3	GD12	VSSQQ	NCOMP	MD2	MD36	MD38	MA13	MA14	CAS0#	CAS1#
AC	AD3	INTA#	AD0	RESETX	VCCQ	SBA6	GD29	VCCQ	GD21	GD18	VCCQ	GD15	GFRAME#	VCCQ	GCLKI	GD9	VCCQ	PCOMP	MD33	MD4	MD6	MD40	CAS5#	MD47	MD15
AD	GREQ#	GGNT#	ST0	SBA0	SB_STB	SBA4	GD31	GD24	GD23	GD17	GDEVSEL#	GTRDY#	GD13	GD10	GD8	GD5	GD4	GD1	MD1	MD35	VSS	MD8	MD10	VSS	MD14
AE	ST2	VSS	SBA1	SBA2	VSS	SBA7	GD27	VSS	AD_STB1	GD19	VSS	GSTOP#	GPAR#	VSS	AD_STB0	GD7	VSS	GD2	MD32	MD3	MD37	MD39	MD41	MD11	MD13
AF	ST1	RBF#	WBF#	SBA3	SB_STB#	GD28	GD25	AD_STB1	GBE3#	AGPVERF	GIRDY#	GBE1#	GD14	GBE0#	AD_STB0	GD6	GD3	GD0	MD0	MD34	MD5	MD7	MD9	MD42	MD43

Additional 36 PWR/GND balls to improve SSO, system stability

Twister System Performance

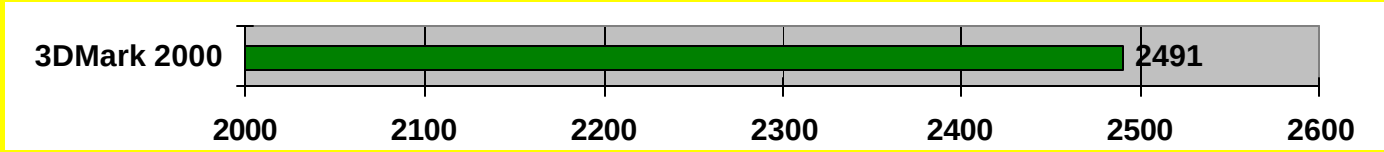


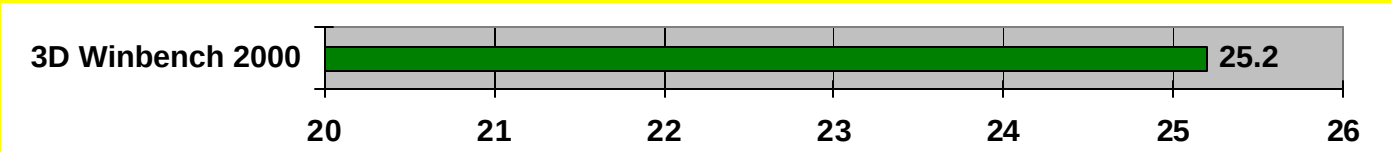
Maximize Memory Bandwidth utilization is Critical in a SMA System

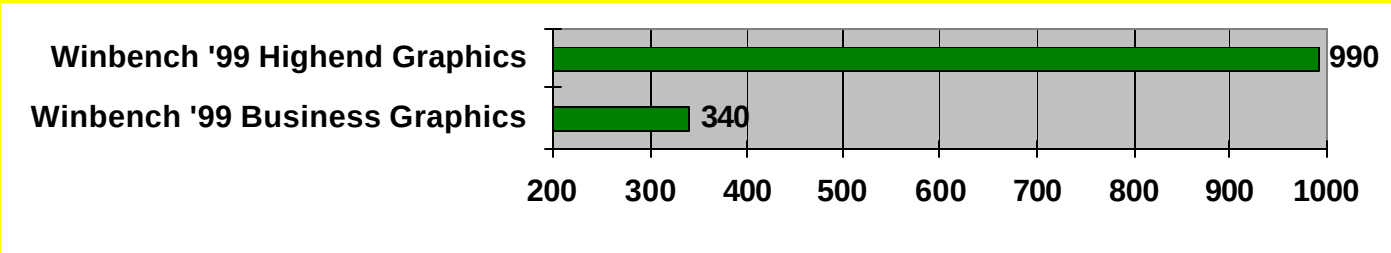
System Configuration:

CPU	**: Pentium III 1GHZ**
M/B	**: VIA Twister motherboard**
VGA	**: On Chip VGA, 16MB shared Memory, 1024x768x16bit**
DRAM	**: 128MB PC-133**
O.S.	**: Windows 98 SE**

Twister Graphics Performance







- **A ideal SMA Graphics Engine needs to have more tolerance of memory latency.**
- **A SMA DRAM Subsystem, requires to handle different DRAM access patterns efficiently**

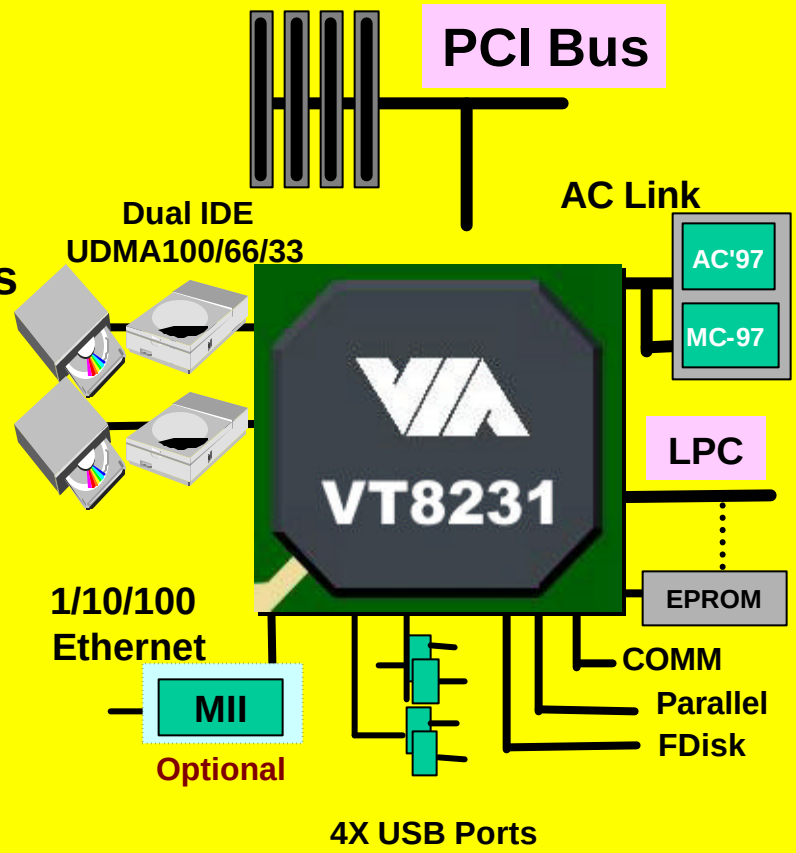
System Configuration:

CPU	**: Pentium III 1GHz**
M/B	**: VIA Twister motherboard**
VGA	**: On Chip VGA, 16MB shared Memory, 1024x768x16bit**
DRAM	**: 128MB PC133**
O.S.	**: Windows 98 SE**

Apollo VT8231 PCI-LPC South Bridge

Highly integrated SB: Networking, Audio, SW Modem, SIO, UDMA100/66, USB and More...

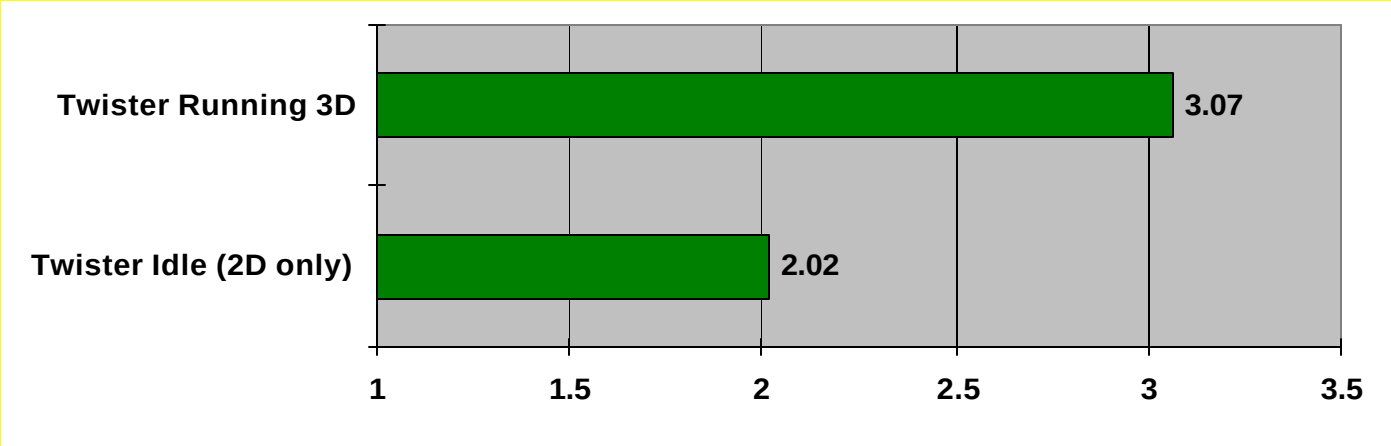
- PCI-LPC South Bridge
- Integrated Networking
  - 10/100 Base-T Ethernet
  - Home PNA
- Hi-Speed Dual IDE controllers
  - ATA100/66/33
- Four (4) USB ports
- Integrated AC'97 Audio, HSP Modem
- Integrated SIO and IO/APIC
- PC99 compliant
- ISA- Less, LPC Interface for optional Ext. SIO and Flash EPROM
- Advanced power management



Enhanced Power Management Support

- **Graphics Enhancements**
  - **BCI Power Management**
    - **3D, MAU, MEU shutdown.**
  - **Gamma, C2 LUT, TV-out power down**
    - **During LCD mode only.**
- **AMD Mobile Athlon support (TwisterK)**
  - **Full support for AMD PowerNow 2.0 technology**
  - **Support for all operating voltage requirements for AMD Duron mobile processors**

Low Power Consumption



Twister Suspend Power <0.08W

***Typical power consumption is the average power consumed while running on Windows 98SE**

Twister is friendly to the mobile system environment

System Configuration:

CPU	: Intel PIII 800/ 133MHz FSB
M/B	: VIA Twister Motherboard
VGA	: On Chip VGA, 8MB shared Memory, 1024x768x16bit
DRAM	: 128MB PC133
O.S.	: Windows 98 SE

Twister Software Support

S3 Graphics and VIA will work together to provide seamless support for customers

- **VIA and S3 are responsible for software development, customer interface, QA, and WHQL**
- **Twister graphic drivers are based on mature drivers from desktop PM/KM133 chipsets**
- **All VIA north bridge and south bridge drivers will work with the Twister family of chipsets**

Summary

- The consolidation of the mobile market require a chipset that can compete in performance at the mainstream market while satisfy cost requirements in the value market
- The Twister family of mobile SMA chipsets is the ideal choice to span these market segments

- Twister + VT8231 provides
  - High integration required to compete in the value segment
  - Performance and high speed memory support to compete in the mainstream market
  - Advanced power management features to meet low power requirements

Back Up

PN133 and KN133 Feature Comparison

Product	ProSavage PN133	ProSavage KN133
North Bridge Features		
CPU Support	Intel PIII/Celeron	AMD Athlon/Duron
CPU Front Side Bus	66/100/133MHz	200/266MHz
DRAM Type	PC100/133	PC100/133
Memory Bus Frequency	100/133	100/133
Max Memory	1.5GB	1.5GB
NB/SB Connection, Bandwidth	PCI, 133MB/s	PCI, 133MB/s
South Bridge Features	VT8231	VT82C686B
IDE Controller	Dual, ATA100/66/33	Dual, ATA100/66/33
AC'97 Audio	Baseline 2 Channels	Baseline 2 Channels
HSP Modem	Yes	Yes
# USB Port	6 Ports/USB1.1	4 Ports/USB1.1
Networking	10/100 Ethernet, Home PNA	No
Super I/O Integration	LPC SIO, KBC, RTC	SIO, KBC, RTC
Expansion Buses	LPC,	ISA
Power Management		
ACPI 1.0/APM 1.2 Compliant	Yes	Yes
AMD PowerNow 2.0 Support	Speedstep	Yes